UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,316	07/11/2003	Patrick Lysaght	X-1410 US	4779

			EXAMINER
24309	7590	01/11/2005	SIEK, VUTHE

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ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/618,316	LYSAGHT ET AL.
	Examiner	Art Unit
	Vuthe Siek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _11 July 2003_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-41_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-8,10-17,19,20 and 22-41_ is/are rejected.

7)☒ Claim(s) _9,18 and 21_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _11 July 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _7/11/03_.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

1.   This office action is in response to application 10/618,316 filed on 7/11//2003.

Claims 1-41 remain pending in the application.

Claim Objections

2.   Claim 32 is objected to because of the following informalities: line 1, "claim 29"

should be changed to --claim 31-- in order to provide proper claimed dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.   Claims 1-8, 10-17, 19-20 and 22-41 are rejected under 35 U.S.C. 102(b) as

being anticipated by Reblewski et al. (6,265,894).

5.   As to claim 1, Reblewski et al. teach a programmable logic device comprising

configurable logic blocks (CLBs) (LEs known as CLBs, Figs. 1, 4a), the CLBs

configured to provide a multi-stage crossbar switch (Fig. 1, 4a, col. 3, 6-7); the multi-

stage crossbar switch including a first stage configured from a first portion of the CLBs

(LEs) to provide a first plurality of crossbars, the first stage having inputs (Fig. 4a); a

second stage configured from a second portion of the CLBs (LEs) to provide a second

plurality of crossbar (Fig. 4a); a third stage configured from a third portion of the CLBs

(LEs) to provide a third plurality of crossbars, the third stage having outputs (Fig. 4a);

first interconnects for coupling the first plurality of crossbars to the second plurality of

crossbars (Fig. 4a); second interconnects for coupling the second plurality of crossbars

to the third plurality of crossbars (Fig. 4a); wherein the inputs and the outputs are

selectable for responsive path configuration to provide input-to-output cross-connectivity

via the first stage, the second stage and the third stage using the first interconnects and

the second interconnects (the multi-stage interconnections crossbars in programmable

logic are dynamically reconfigurable network for routing path between inputs and

outputs) (see at least col. 6-8).

6.   As to claim 22, remarks set forth in rejecting claim 1 equally apply because of

similar claimed limitations.

7.   As to claim 28, remarks set forth in rejecting claim 1 equally apply. Note that the

multi-stage crossbars as taught by Reblewski et al. are dynamically reconfigurable for

routing between selectable inputs and outputs (the cross-connectivity is reconfigurable)

(see at least col. 8).

8.   As to claim 31, remarks set forth in rejecting claim 1 equally apply. Note that the

multi-stage crossbars as taught by Reblewski et al. have three stages (col. 6, lines 66-

67).

9.   As to claim 34, remarks set forth in rejecting claim 1 equally apply. . Note that

the multi-stage crossbars as taught by Reblewski et al. are dynamically reconfigurable

for routing between selectable inputs and outputs (the cross-connectivity is

reconfigurable) (see at least col. 6-8). The dynamically reconfigurable network enable

user to reconfigurably route a selective subset of state values for up to 32 LEs (CLBs) to

partial scan register. So the crossbar switch network within the PLD is dynamically

reconfigurable by providing predefined configuration bits and access to user.

10.   As to claims 36 and 38, remarks set forth in rejecting claim 1 equally apply. In

addition, Reblewski et al. the multi-stage crossbars network comprises processor on a

single chip (col. 3, lines 9-44, col. 10 lines 10-25). So a processor is embedded within

the single chip PLD.

11.   As to claim 2, Reblewski et al. teach a multi-stage crossbars (three stages) for

selectively routing signal between inputs and outputs (Figs. 1, 4a).

12.   As to claim 3, Reblewski et al. teach the first plurality of crossbars are interleaved

with the third plurality of crossbar (Fig. 4a), where the second crossbar is disposed

there between.

13.   As to claim 4, Reblewski et al. teach the first interconnects and the second

interconnects are disposed in an interconnect region, and the second crossbars are

disposed within the interconnection region (Fig. 4a), where the second crossbars are

disposed between the interconnection region.

14.   As to claim 5, Reblewski et al. teach the first crossbars and third crossbars are

not disposed within the interconnect region (Fig. 4a), where the first crossbars and third

crossbars are disposed outside the interconnect region.

15.   As to claim 6, Reblewski et al. teach the second crossbars are arrayed (Fig. 4a).

16.   As to claims 7, 10-15, 16, 19 and 23-26, Reblewski et al. teach each crossbar of

the first crossbars/second crossbars/third crossbars comprises a first set of the first

portion of CLBs (LEs) configured to provide input flip-flops and a second set the first

portion of the CLBs (LEs) configured to provide multiplexers (MUXs) and output flip-flops (Figs. 8a-8b). Note that each crossbar pipelines data from an input register stage to a multiplexer stage and to an output register stage for the multi-stages crossbar network through dynamically reconfigurable network including full scan chain/partial scan chain and multiplexers for reconfiguring the crossbars network by user (Figs. 1, 4a, 8a-8b, col. 6-8).

17.   As to claim 8, 17 and 20, Reblewski et al. teach outputs of the input flip-flops are selectively coupled to and uncoupled from function generators (MUXs) through partial reconfiguration (partial scan chain of dynamically reconfigurable network) (Figs. 8a-8b), where the MUXs are selectively inputs of flip-flops).

18.   As to claim 27, Reblewski et al. teach implementing a multi-stages crossbars within a single chip (PLD, FPGA) comprising a processor and dynamically reconfigurable network of scan chain/partial scan chain and multiplexers (col. 1, 3, 7, 8, 10). The dynamically reconfigurable network includes modifying the configuration information.

19.   As to claims 29-30, 32-33 and 35, Reblewski et al. teach a multi-stages crossbars for selectively routing signal by user between inputs and outputs, where each crossbar comprises dynamically reconfigurable network including scan chain/partial scan chain, selectors and function generators (MUXs) under configuration bit control (Figs. 8a-8b, col. 8), where the scan chain is operable through scan clock, therefore latency from any of the input pins cross-connected to any of the output pins is a same number of clock cycles.

20.   As to claim 37, Reblewski et al. teach a multi-stage crossbars (three stages

crossbar network) that is dynamically reconfigurable (Figs. 1, 4a, col. 8)

21.   As to claim 39, Reblewski et al. teach a multi-stage crossbars comprising

configurable interconnects coupling inputs of the multi-stage crossbar switch to outputs

of the multi-stage crossbars switch (Fig. 4a).

22.   As to claims 40-41, Reblewski et al. the single chip comprises a multi-stage

crossbar and processor (hard processor, general-purpose processor) (col. 10, lines 10-

25)

Allowable Subject Matter

23.   Claims 9, 18 and 21 are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims. The prior art does not teach

double-length lines connected to the outputs of the input flip-flops; and programmable

input select circuitry configured to selectively couple and uncouple function generators

to and from the double-length lines; selectively couple and uncouple to lookup tables

and from the double-length lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

· VUTHE SIEK
PRIMARY EXAMINER